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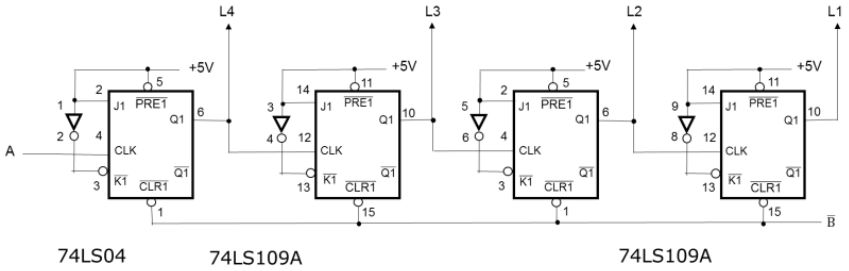
Wednesday lab session 12:00-3:00

Experiment #4: Binary Counters and Shift Registers

Aim: Practice implementation of asynchronous and synchronous binary counters and shift registers

Results:

1. We began by connecting up the asynchronous binary counter shown below using 74LS109A and 74LS04 IC packages.



2. We proceeded to toggle the clock switch several times to light up a couple of the LED's. We then pressed switch B' then released it again and found that the counter changed when B' went from low to high, which made the input CLR' go high.

3. Next, we created the truth table shown below for the outputs of L1-L4 after each pulse of A. We found that the counter state changed on the rising edge of A and the circuit functioned as a binary down counter.

Pulse #	L1	L2	L3	L4
0	0	0	0	0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1

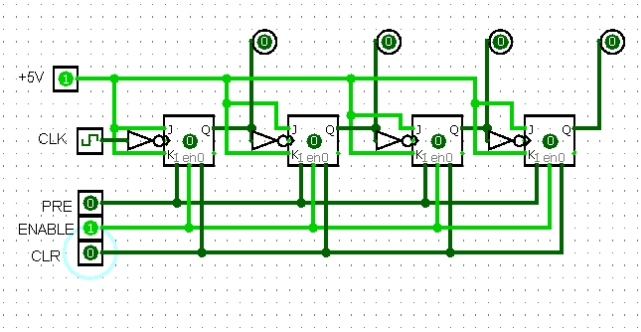
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

4. For step four we connected the clock switch to a 1 hz counter and noted the result of pressing switch B' at different points in the clock cycle. We found that the timing doesn't matter and whenever B' is pressed, all output values go low. We also found that if B' is held down then the clock pulses have no effect on the counter.
5. We then modified our circuit to function as an up counter by changing the clock inputs to CLK' instead of CLK. We then checked it with a truth table. The circuit and truth table are shown below.

Pulse #	L1	L2	L3	L4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1

14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

Pulse #	L1	L2	L3	L4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0



6. Next, used the 74LS109A, 74LS08, and 74LS04 IC packages we wire up the synchronous binary counter shown below and recorded a truth table of its outputs after each pulse. We found that it functions as a modulo-16 binary up counter.

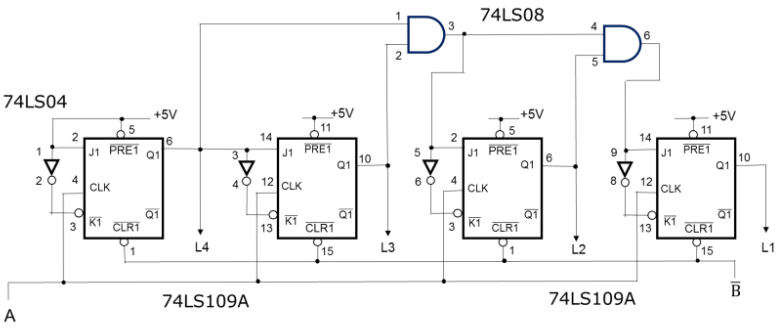
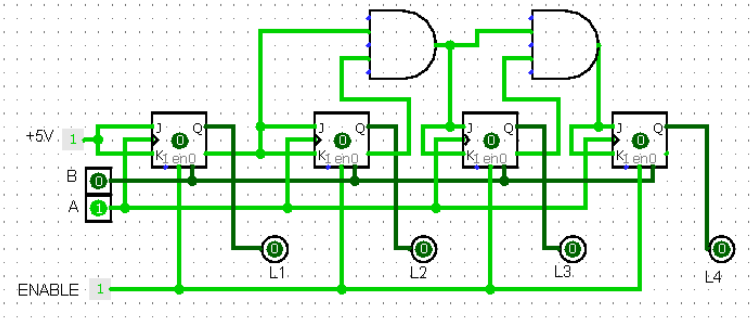


Fig 2.

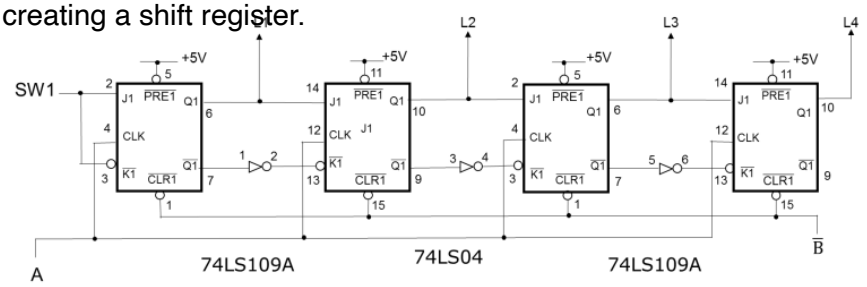
7. We proceeded to explore how to modify the circuit above to function as a down counter. Our solution was to change the input of each flip flop to the Q' output of the previous flip flop instead of Q. The new circuit and verifying truth table are shown below.

Pulse #	L1	L2	L3	L4
0	0	0	0	0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0



13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

8. For this step, we used the 74LS109A and 74LS04 IC packages to wire up the circuit below, creating a shift register.

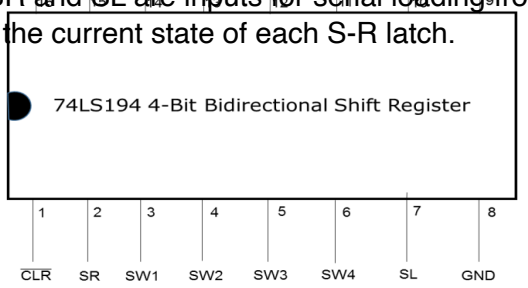


9. We then tested the circuit by first pressing B' to clear all the outputs, then setting SW1 to high and giving 4 clock pulses, and finally setting SW1 to low and giving 4 more clock pulses. The results are recorded in the table below.

SW1	Pulse #	L1	L2	L3	L4
	0	0	0	0	0
1	1	1	0	0	0
1	2	1	1	0	0
1	3	1	1	1	0
1	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0

10. We found that to load the value 0101 (L1-L4), you must turn on SW1, give one clock pulse, turn SW1 off, give the next clock pulse, turn SW1 back on, give a third clock pulse, and finally turn SW1 off again and give a fourth clock pulse.

11. Next, we wired up the circuit according to the diagram below using the 74LS194 IC package. The selector lines S1 and S0, are used to select the following functions: 11 = parallel load, 01 = shift right, 10 = shift left, 00 = inhibit clock. SW1-SW4 are inputs when using parallel load, SR and SL are inputs for serial loading from the left and right, and L1-L4 are outputs of the current state of each S-R latch.



12. We then set S1 = S0 = 1 and SW1-SW4 = 1, and applied a single clock pulse. The resulting output was L1-L4 all lighting up as the inputs were loaded in parallel to the S-R latches. As is depicted in the diagram below, when S0 and S1 are both high, the multiplexors for the input of each S-R latch select the values of SW1-SW4 as direct inputs.

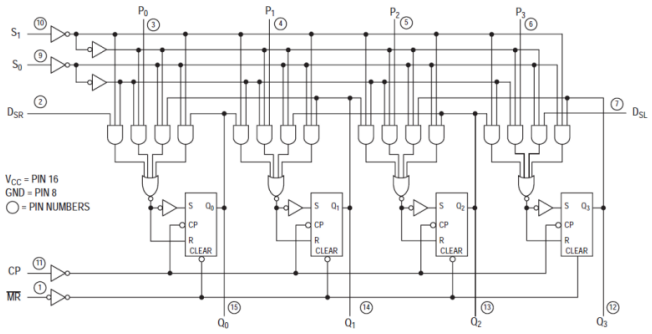


Fig. 5

13. Following this, we cleared all outputs by connecting pin 1 (CLR') to GND and then back to +5v.

14. We then used SW1-SW4 to load the value 0101 to the outputs of the four S-R latches and set S1 = 0 and S0 = 1 as well as pin 2 (SR) to 1. We applied three clock pulses and noted the outputs after each one in the table below.

Pulse #	Q0	Q1	Q2	Q3
0	0	1	1	1
1	1	0	1	0
2	1	1	0	1
3	1	1	1	0

15. For this step we cleared all outputs again by briefly setting CLR' to GND, then set S0=S1=1 and used SW1-SW4 to parallel load 1000 to outputs Q0-Q3. We changed S1 to 1 and S0 to 0, along with setting pin 7 (SL) to 1, and then applied three clock pulses and noted the outputs after each one in the table below.

Pulse #	Q0	Q1	Q2	Q3
0	1	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1

16. For the final step we parallel loaded values 1000 in the same way as before. We then set S1=S0=0 and toggled the clock input several times. We found that the outputs did not change while S1 and S0 were set to 0. This is because the multiplexors shown in the figure from step 12 use the output of each S-R latch as the input for the same latch. This creates a closed cycle and keeps each value consistent no matter how many clock pulses are given.

Discussion: The errors we ran into in this lab mostly involved faulty equipment. For example, at one point we had an LED that was wired up correctly but wouldn't light up. We fixed this problem by using Logisim when necessary to confirm the results from our physical circuit. Other than this we came to confident conclusions about all our results.

Conclusion: In this lab, we gained experience working with synchronous and asynchronous up/down counters and began to build more complex circuits that could serve multiple functions. We worked with shift registers and began to see how these tools could be used to serve practical functions, especially when coupled with things like multiplexors. We came away feeling good about our results and considered the experiment as a whole a success.